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Title : PIT REDUCTION SYSTEM

2.CLAIMS

A bit reduction system for converting an analog input signal to a digital signal by an A/D converter of n bits (n is an integer not less than 2);

Adding a dither data with a predetermined frequency, which is equivalent to a lower side d (d is an integer of $1 \leqq d < n$) bits including at least LSB and is in accordance with a clock of said A/D converter to the n bits output data from said A/D converter; and

transmitting a digital signal of (n-d) bits, in which the lower side d bits of this addition output data are cut off.

In this FIG. 1, an input terminal 1 is provided with a signal such that an analog-video signal or a digital-video signal is once D/A converted. This input analog signal is transmitted to an A/D converter 3 of 8 bits (generally, n bits) via a LPF (low-pass filter) 2 for an anti-aliasing. This A/D converter 3 is activated by a clock signal of a frequency fc (a frequency Tc) from a clock generating circuit 4. This clock

signal becomes a rectangular wave signal of a frequency fc/2 (a frequency 2Tc) by a 1/2 frequency divider to be transmitted to an adder 6. This rectangular wave signal comprises a binarized signal of 1 bit such that 1, 0 are alternately shown for every the above clock frequency Tc (namely, 2Tc frequency). This rectangular wave signal is added (carry addition) by the adder 6 to the data of 8 bits from the A/D converter 3 as the data of a LSB (the lowest bit). The addition data of 8 bits from the adder 6 is made into 1/2 value by a divider 7 such as a bit-shifter or the like to be taken out from an output terminal 8. Specifically, this is an operation for cutting off the LSB of the data of 8 bits (generally, n bits) and taking out the remaining 7 bits (generally, n-1 bit). The data from the output terminal 8, of which bits are reduced in this way, is transmitted. In other words, it becomes possible to transmit the video data of 8 bits via a transmission path of 7 bits.

FIG. 1 is a block circuit diagram for illustrating a bit reduction system of an embodiment according to the present invention.

FIG. 1

EXPLANATORY VIEW OF AN EMBODIMENT

3: A/D CONVERSION (N BITS)

4: GENERATION OF CLOCK

5: 1/2 FREQUENCY DIVISION

6: ADDITION

7: 1/2 (CUT OFF LSB)